

# SPICE Simulation and Tradeoffs of CMOS LNA Performance with Source-Degeneration Inductor

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*Abstract*— In this paper, we study the tradeoffs of CMOS LNA using source-degeneration inductor with both experimental data and simulation (MEDICI) data. SPICE models based on the quasi-static (QS) assumption ignores the channel resistance and leads designers to overly rely on source-degeneration inductance. The non-QS (NQS) model is much better. Source inductor adversely affects noise and gain. The parasitic capacitance at the gate imposes additional challenges for matching.

## I. INTRODUCTION

IN CMOS low noise amplifier (LNA) circuits, matching is often done with a source-degenerative inductor [1]. When referred back to the gate input, the source-degenerative inductance is transformed into a real impedance. The advantage of using the source-degenerative inductor is that it ideally does not introduce extra noise source. In SPICE simulation, designers often over-estimate the amount of matching required.

In most of the popular CMOS models used in SPICE, a quasi-static (QS) model is assumed. The QS model assumes no channel resistance. In high speed digital applications, the absence of channel resistance, in particular the distributive nature of it, leads designers to predict transient behavior inaccurately, as detailed in [2]. In RF application, the model leads designers to underestimate the input impedance [3].

In this paper, we first quantify the channel resistance. The study uses a device simulator based on an industrial deep-submicron *lightly doped drain* (LDD) structure. It is followed by measurement of a fabricated LNA. Both QS and NQS models are scrutinized. After that, we proceed to study the by-products of having source-degenerative inductors. While the study is valid across a wide range of frequencies, the second part of this paper focuses mainly on the 2.4 GHz spectrum. The 2.4 GHz is the second lowest ISM band in the United States, and it is the first high frequency, wideband license-free frequency spectrum in places such as Hong Kong.

## II. FINITE CHANNEL RESISTANCE

We use noiseless resistor  $R_{ch}$  to account for the intrinsic resistance seen at the gate due to the finite charging time of the carriers in the inversion layer [2]. Unlike the noisy gate-poly parasitic resistance  $R_g$  (Fig. 1), the channel resistance  $R_{ch}$  cannot be reduced using layout techniques. ‘Fingering’ the gate-poly only reduces  $R_g$ . From real measurement,  $R_g$

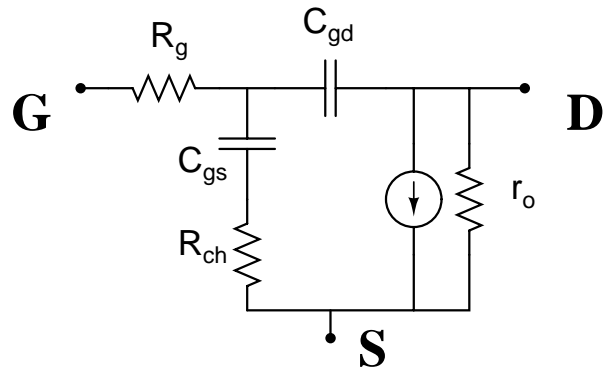


Fig. 1. Small signal model of MOSFET including the intrinsic channel resistance  $R_{ch}$  and parasitic gate-poly resistance  $R_g$ .

and  $R_{ch}$  cannot be easily distinguished. As such, we examine the extent of the channel resistance first through simulation of a  $0.35 \mu\text{m}$  LDD NMOS with doping profile similar to that published in [4]. The processing steps were simulated with TSUPREM, through which essential features of the transistors were extracted:  $t_{ox} = 7.6 \text{ nm}$ , drain/source doping =  $1.3 \times 10^{21} \text{ cm}^{-3}$ , drain/source junction depth =  $0.15 \mu\text{m}$ , LDD doping =  $1 \times 10^{20} \text{ cm}^{-3}$ , LDD junction depth =  $0.05 \mu\text{m}$ , and substrate doping  $6.2 \times 10^{14} \text{ cm}^{-3}$ . The extracted device was then simulated with MEDICI. A substrate depth of  $5 \mu\text{m}$ , rather than a full wafer depth of hundreds of  $\mu\text{m}$ , was simulated. However, the epi-substrate nature of the process would guarantee that the omitted depth is mostly highly doped and will not severely affect the results [5]. A frequency sweep from 1 GHz to 26 GHz was performed on the device. To avoid the output loading effect, the input impedance is calculated from the Y-parameters. The results are displayed in Fig. 2. The real part of the input resistance is between 10 to  $12 \Omega$  for a  $50 \mu\text{m}$  wide device.

In addition, to take advantage of this intrinsic device, we used a SPICE model parameter extractor<sup>1</sup> to extract the BSIM3v3 model of the device from the MEDICI data. Both the QS and the NQS behavior were then simulated using the freely available Berkeley SPICE and BSIM3v3 source code from UC Berkeley<sup>2</sup>. (The HSPICE simulator does implement the BSIM3v3 as MOS model level 49, but does not support the NQS effect.) The results are also plotted in Fig. 2. The QS model assumes no channel re-

<sup>1</sup>Bsim Pro, BTA Corp.

<sup>2</sup>BSIM3 is developed by the Device Research Group of the Department of Electrical Engineering and Computer Science, University of California, Berkeley and copyrighted by the University of California. <http://www-device.eecs.berkeley.edu/~bsim3/>

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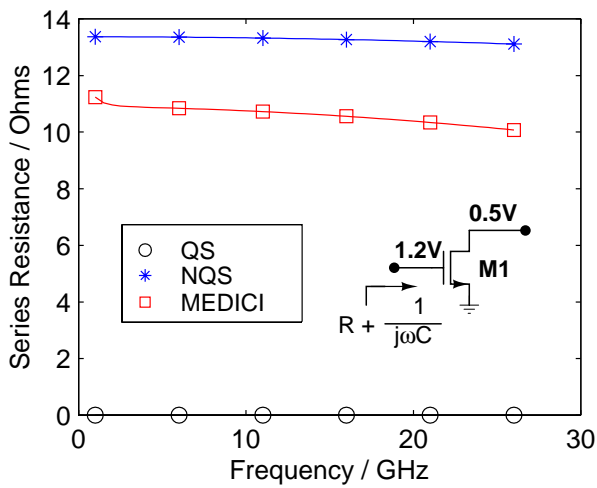


Fig. 2. The real part of input impedance of transistor M1 when the drain is AC shorted to ground.

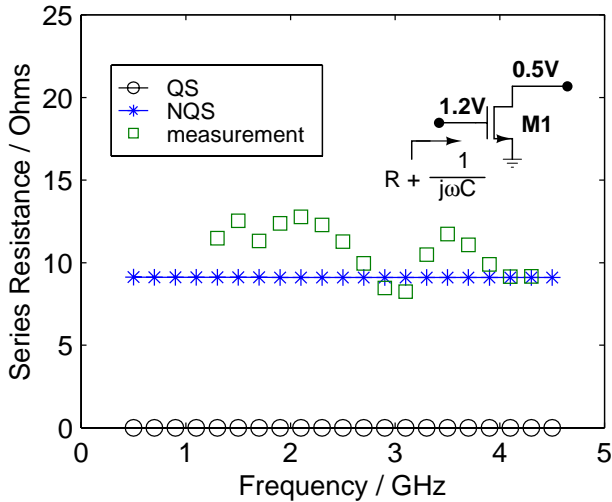


Fig. 3. The real part of input impedance of the NMOS device when the drain is AC grounded. The measurement result is de-embedded using dummy device.

sistance and reflects no input series resistance across the entire frequency range. The NQS models the channel resistance better than the QS version but still overestimates the value by slightly more than  $3\ \Omega$ .

A  $50\ \mu\text{m}/0.35\ \mu\text{m}$  device was fabricated using the HP process obtained through MOSIS. MOSIS provides a set of BSIM3 parameters [6]. In Fig. 3, we show both the measurement results and the SPICE simulation results with both QS and NQS models. The high frequency characteristic of the device is comparable to the previous MEDICI simulation although no special effort was made to match these two independent processes. The measured input impedance is between  $8$  to  $13\ \Omega$ . The  $R_g$  here is less than  $1\ \Omega$  due to gate-poly fingering.

### III. LNA IMPEDANCE MATCHING

From both device simulation and measurement, we found that there exists more than  $10\ \Omega$  of real impedance looking into the gate of MOSFET under bias. This finite resistance

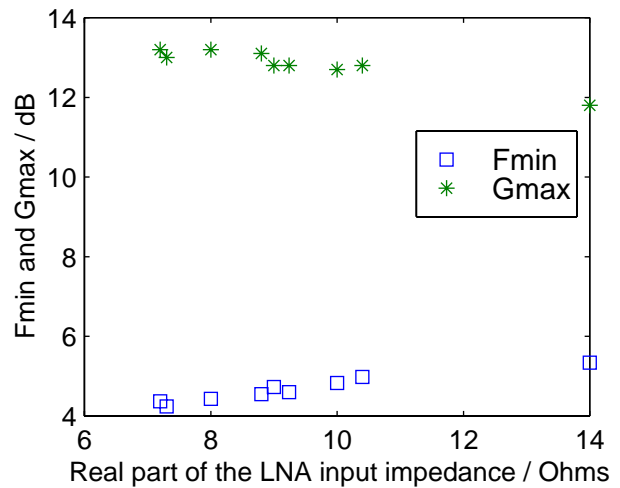


Fig. 4. Measured  $F_{min}$  and  $G_{max}$  of the LNA at 2.4GHz for different source bondwire inductance. This noise matched  $F_{min}$  set the lower bound of minimum noise figure can be achieved under power matched condition.

is significant at high frequency but ignored in most cases, especially when model based on the QS assumption is used.

Using source-degeneration inductor to solely support the need for real part input matching is not necessary. We can make use of the channel resistance to augment the input resistance. What is of interest is how much should we still rely on the source-degeneration inductance and what are the impacts on the LNA performance. These are studied experimentally and discussed in the following section.

A cascode LNA input stage was fabricated using a  $0.35\ \mu\text{m}$  CMOS technology. The width of the input transistor M1 of the LNA is  $50\ \mu\text{m}$ . The source inductor value was changed by attaching different bondwires. The minimum noise figure ( $F_{min}$ ) and available gain ( $G_{max}$ ) for noise match were measured using an ATN NP5 system. The results are plotted against the real part of the input impedance in Fig. 4. The real part of the input impedance is changed when the source inductors are changed.

### IV. DISCUSSIONS

The use of source inductor impacts the LNA performance in several ways. The additional resistance synthesized from the source inductor reduces the Q-factor of the LNA input network and hence degrades the amplifier gain. Using the small signal model which includes the channel resistance (Fig. 5), we can deduce the effective transconductance ( $i_o/v_s$ ) at resonance using gate inductor  $L_g$  (discussed later) and source inductor  $L_s$ .

$$G_{m,eff} = g_m Q_{in} = \frac{\omega_T}{\omega_o (R_s + R_{ch} + \omega_T L_s)} \quad (1)$$

Here  $Q_{in}$  is the input Q-factor of the LNA.  $\omega_o$  and  $\omega_T$  are the resonant and unity-gain frequencies respectively, and  $R_s$  is the antenna impedance real part. Also, assume the source inductor has very high Q. Imposing the maximum power transfer constraint, i.e.  $R_{ch} + \omega_T L_s = R_s$ , equation (1) becomes

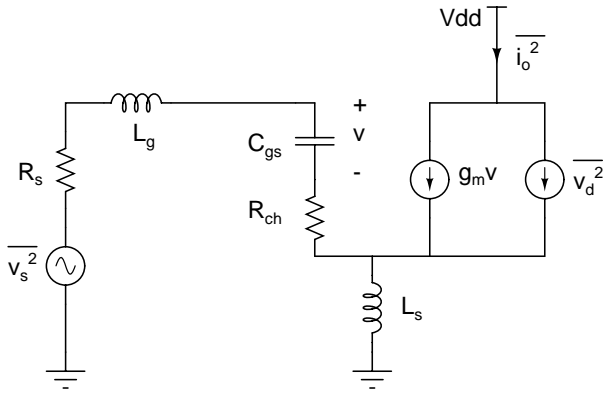


Fig. 5. Small signal model including channel resistance for both LNA effective transconductance and noise figure calculation.

$$G_{m,eff} = \frac{\omega_T}{2\omega_o(R_{ch} + \omega_T L_s)} \quad (2)$$

The effect of varying source resistance  $R_s$  on the LNA performance can be seen from the ratio of output current square  $i_o^2$  to power  $P_s$  available from the antenna. Under the constant available power constraint, the source voltage varies as the source resistance and equals  $2\sqrt{P_s R_s}$ . The ratio is then,

$$\frac{i_o^2}{P_s} = G_{m,eff}^2 \frac{v_s^2}{P_s} = \frac{\omega_T^2}{\omega_o^2(R_{ch} + \omega_T L_s)} \quad (3)$$

An increase in  $L_s$  decreases the output current  $i_o$  for given input power. Maximum  $i_o$  is achieved when  $L_s$  is zero, in which case,

$$\left. \frac{i_o^2}{P_s} \right|_{max} = \frac{\omega_T^2}{\omega_o^2 R_{ch}} \quad (4)$$

The impact of  $L_s$  on noise figure is not so obvious at first glance as the source inductor suppresses both the output noise current due to negative feedback and the output signal. The net effect on the signal-to-noise ratio depends on which decreases faster. Using the same small signal model and assuming a drain noise current power spectral density of  $4KT\gamma g_{d_o}$ , we have derived the noise figure when maximum power transfer is achieved at resonance:

$$F = 1 + \gamma g_{d_o} \frac{(2R_{ch} + \omega_T L_s)^2}{R_{ch} + \omega_T L_s} \left( \frac{\omega_o}{\omega_T} \right)^2 \quad (5)$$

Again, the minimum noise figure is achieved when there is no source inductance. The corresponding minimum noise figure is

$$F_{min} = 1 + 4\gamma g_{d_o} R_{ch} \left( \frac{\omega_o}{\omega_T} \right)^2 \quad (6)$$

In both equations (4) and (6), the assumption here is that  $L_s$  is equal to zero. Or, from another perspective, these equations require the source impedance,  $R_s$ , from the stage preceding the LNA to match exactly with  $R_{ch}$ . In most systems, the stage preceding an LNA is a discrete

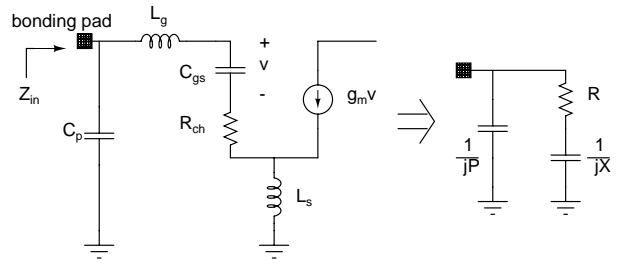


Fig. 6. Undesirable downward impedance transformation results from parasitic capacitance at the LNA input.

dielectric filter whose impedance is  $50 \Omega$ . Since  $R_{ch}$  from both measurement and simulation are still far from  $50 \Omega$ , external matching network at the gate will be required to completely eliminate  $L_s$ . It is only fair to acknowledge that any additional matching network at the gate will bring in other complications due to their finite Q's. Nonetheless, the above equations represent an ideal theoretical limit.

Relying on the source inductor completely to fulfill the  $50 \Omega$  real input impedance may also be more difficult than expected. As shown in Fig. 6, there exists some parasitic capacitance  $C_p$  from the LNA input to the ground. This capacitance can be from a bonding pad, for instance.  $C_p$  helps downward transform  $L_s$  when referred back to the input. Referring to Fig. 6, define the following:

$$\begin{aligned} R &= R_{ch} + \omega_T L_s \\ \frac{1}{jX} &= \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) \\ \frac{1}{jP} &= \frac{1}{j\omega C_p} \end{aligned} \quad (7)$$

where  $L_g$  indicates a possible on-chip gate circuit inductor for matching. The real part of the input impedance,  $Z_{in}$ , is then

$$Re\{Z_{in}\} = \frac{R}{(RP)^2 + (1 + \frac{P}{X})^2} < R \quad (8)$$

Here, we notice that  $Re\{Z_{in}\}$  is downward transformed from  $R$  by a factor. The reduction increases as parasitic capacitance  $C_p$  increases. Moreover, if  $Re\{Z_{in}\}$  is plotted against  $L_s$ , there exists a maximum  $Re\{Z_{in}\}$  at certain  $L_s$ . Beyond that,  $Re\{Z_{in}\}$  does not increase any further despite further increase in  $L_s$ . This particular value of  $L_s$  depends on frequency and  $C_p$  (Fig. 7).

In Fig. 7, we portray three cases for discussion. In all three cases, we assume an operating frequency of 2.4 GHz,  $C_{gs} = 90$  fF,  $R_{ch} = 10 \Omega$ , and  $\omega_T = 2\pi \times 9 \times 10^9$  rad/sec. In the first case, we plot the  $Re\{Z_{in}\}$  assuming no parasitic capacitance  $C_p$ . In this case (curve a), the  $Re\{Z_{in}\}$  increases monotonically since  $Re\{Z_{in}\} = R_{ch} + \omega_T L_s$ . In the second case, we take  $C_p$  into consideration. In addition we include an on-chip spiral inductor,  $L_g$ , to be added at the gate to augment the matching. However, we assume that the designers are oblivious to  $C_p$ . In the design, the choice of  $L_g$  and  $L_s$  are only done to tune out  $C_{gs}$ , the gate source capacitance of the input stage. With  $L_g$  and  $L_s$  set, we simulate the  $Re\{Z_{in}\}$  with  $C_p$ . We show in curve (b) that in order to achieve  $50 \Omega$ ,  $C_p$  cannot be

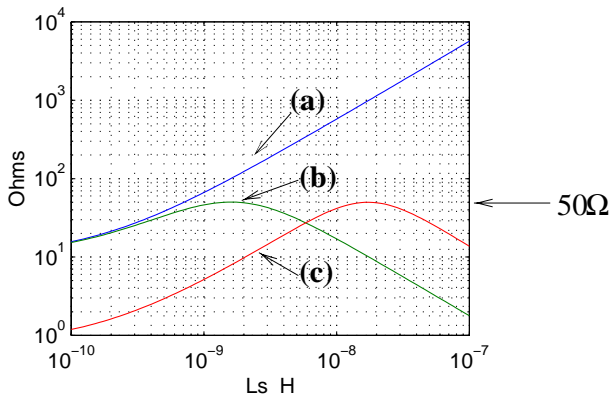


Fig. 7. Real part of input impedance in Fig. 6 at 2.4 GHz. Curve (a) shows the expected resistance ( $R_{ch} + \omega_T L_s$ ). Curve (b) shows the case of on-chip matching ( $1/X = 0$ ) and  $C_p = 0.66$  pF. Curve (c) shows the case of off-chip matching ( $L_g = 0$ ) and  $C_p = 0.237$  pF.

larger than 0.66 pF. In the last case, we assume no  $L_g$ . Instead, we use external discrete matching to supplement  $L_s$ . Thus,  $C_p$  will be in-between the discrete matching network and the gate node. Curve (c) shows that the critical  $C_p$  is 0.237 pF, roughly twice the capacitance of a bonding pad. Beyond that,  $Re\{Z_{in}\}$  cannot be larger than 50  $\Omega$ . Note that although  $C_p$  is smaller in the last case which is the most common situation,  $Re\{Z_{in}\}$  is much smaller than the second case.

Equation (8) shows that in any event, the required source inductor is larger than that predicted when no  $C_p$  is assumed. This additional source inductance will further degrade the LNA performance as shown in equations (3) and (5).

## V. CONCLUSION

The existence of the channel resistance was shown from both MEDICI simulation and device measurement. This resistance was usually overlooked by designers who were looking for real impedance for impedance matching to antenna. Analysis and measurement showed that both noise and gain performance of LNA are improved by reducing source inductance. We can safely eliminate the source inductor completely and rely on the channel resistance for impedance matching. Furthermore, on-chip matching LNA input to 50  $\Omega$  is not recommended as more source inductance is needed to compensate the input pad parasitic capacitance.

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## REFERENCES

- [1] D. K. Shaeffer, T. H. Lee, "A 1.5V, 1.5 GHz CMOS low noise amplifier", *IEEE Journal of Solid State Circuits*, May 1997, pp. 745-759.
- [2] Mansun Chan, Kelvin Y. Hui, Chenming Hu, Ping K. Ko, "A robust and physical BSIM3 non-quasi-static transient and AC

small-signal model for circuit simulation", *IEEE Transaction on Electron Devices*, vol. 45, April 1998, pp. 834-841.

- [3] Jia-Jiunn Ou, Xiaodong Jin, Ingrid Ma, Chenming Hu, Paul R. Gray, "CMOS RF modeling for GHz Communication IC's", *Symposium on VLSI Technologies, Digest of Technical Papers*, 1998.
- [4] Masanobu Saito, Mizuki Ono, Ryuichi Fujimoto, Hiroshi Tanimoto, Nobuyuki Ito, Takashi Yoshitomi, Tatsuya Ohguro, Hisayo Sasaki Momose, Hiroshi Iwaii, "0.15  $\mu$ m RF CMOS technology compatible with logic CMOS for low-voltage operation", *IEEE Transaction on Electron Devices*, vol. 45, March 1998, pp. 737-742.
- [5] Alan L. L. Pun, Tony Yeung, Jack Lau, Francois J. R. Clement, David Su, "Substrate Noise Coupling through Planar Spiral Inductor", *IEEE Journal of Solid State Circuits*, June, 1998, vol. 33, no.6, pp. 877-884.
- [6] World wide web homepage address: <http://www.mosis.org/cgi-bin/params/hp-gmos10qa/n7cu.prm>